INTEL® XEON PHI™ COPROCESSOR Case Study

Software Ecosystem Snapshot and End User Momentum
HOW TO EVALUATE YOUR APPLICATION
EVALUATING YOUR APPLICATIONS

Can your workload scale to over 100 threads?

NO

Can your workload benefit from large vectors?

NO

Can your workload benefit from more memory bandwidth?

NO

YES

Use Intel® Xeon Phi™ coprocessors for applications that scale with:

• Threads
• Vectors
• Memory Bandwidth

Click to see Animation video on Exploiting Parallelism on Intel Xeon Phi Coprocessors

Representative example workload for illustration purposes only
BREAKTHROUGH PROGRAMMING EFFICIENCY
For Accelerating Highly Parallel Applications

Maintain a single code base
- Software that runs on Intel® Xeon® processors also runs on Intel® Xeon Phi™ coprocessors

Use familiar tools
- No need to learn new tools, languages, or development models

Optimize code just once
- Optimizations for Intel® Xeon Phi™ coprocessors also boost performance for Intel Xeon processors

Preserve your investment
- Don’t reinvent the wheel—accelerate performance for existing applications
FLEXIBLE USAGE MODELS

SOURCE CODE

Compilers, Libraries and Parallel Models

Highly parallel code
Serial and moderately parallel code

Execution Models

Percentage of Code

Multicore Only (90% of applications)

Multicore Hosted with Manycore Offload

Symmetric

Manycore Only

MAIN ()

XEON(s)

MAIN ()

XEON(s)

Xeon Phi(s)

MAIN ()

XEON(s)

Xeon Phi(s)

MAIN ()

Xeon Phi(s)
## Examples of Highly Parallel Market Segments & Applications

Click on links for more information

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<td>RTM (Reverse Time Migration), WEM (Wave Equation Migration)</td>
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<td>(Molecular Dynamics,</td>
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### Mix of ISV and End User Development
A GROWING ECOSYSTEM:
Developing today on Intel® Xeon Phi™ coprocessors

Shown at SC’12, November 2012
## Intel® Xeon Phi™ Coprocessor: Performance Proof-points
Click on links for more information (SC12)

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<td>Overflow (NASA, Symmetrec)</td>
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CFD Application

- **ANSYS Fluent status:**
  - ansys Fluent has been trying to do a “beta” release of Fluent for Xeon Phi.

- **OpenFOAM:**
  - The current status is that OpenFOAM is about 2x slower on KNC compared to SNB-EP 2S, 1600 MHz. This is single-node, so no Infiniband involved.
  - open source development team did not want to do anything to customize for Phi.

- **Overflow (NASA):** NASA Overflow has done the best of known structured solvers.

- **StartCD|StartCCM+:** Ongoing.
Case Study: TACC -- LBM
Porting to the Intel Xeon Phi: Opportunities and Challenges

Carlos Rosales

carlos@tacc.utexas.edu
Motivation and main algorithm characteristics

THE LATTICE BOLTZMANN METHOD
Programming Models

• Traditional Cluster
  – Pure MPI and MPI+X
    • X: OpenMP, TBB, Cilk+, OpenCL, ...

• Native Phi
  – Use one Phi and run OpenMP or MPI programs directly

• MPI tasks on Host and Phi
  – Treat the Phi (mostly) like another host
    • Pure MPI and MPI+X

• MPI on Host, Offload to Xeon Phi
  – Targeted offload through OpenMP extensions
    – Automatically offload some library routines with MKL
Code Structure

- Collision: Local calculation. Most of the math takes place here.
- PostCollision: Boundary corrections for outward f values
- Stream: Move collision data along velocity directions
- PostStream: Boundary corrections for inward f and g

TACC
THE UNIVERSITY OF TEXAS AT AUSTIN
TEXAS ADVANCED COMPUTING CENTER
Governing equations

Navier-Stokes

\[ \frac{\partial (n \mathbf{u})}{\partial t} + \nabla \cdot (n \mathbf{u} \mathbf{u}) = -\nabla P + \mu \nabla^2 \mathbf{u} + \mathbf{F}_b \]

Mass Conservation

\[ \frac{\partial n}{\partial t} + \nabla \cdot (n \mathbf{u}) = 0 \]

Cahn-Hilliard

\[ \frac{\partial \phi}{\partial t} + \nabla \cdot (\phi \mathbf{u}) = \theta_M \nabla^2 \mu_\phi \]

Chemical Potential

\[ \mu_\phi = 4\alpha \left( \varphi^3 - \varphi^2 \varphi \right) - \kappa \nabla^2 \varphi \]
Challenges

• Industrially Relevant
  – Density and viscosity ratios
  – Volume fractions
  – Poly-disperse suspensions

• Capture the Physics
  – High time/space resolution
  – Large data sets
    • Storage
    • Visualization
PORTING THE LBM CODE
Setting Expectations

- Performance ratios between one mic and two E5-2680 sockets:
  - In FP Ops: $1074 / 345 = 3.1x$
  - In Memory BW (approx): $180 / 80 = 2.2x$

- So, the best acceleration I can expect is:
  - 3.1x for fp bound code
  - 2.2x for memory bw bound code

- And most likely I will get something in between these two results.
Original Code

- Multiphase LBM based on Free Energy formulation
- Single 4D array for f and single 4D array for g
- Double-buffered to avoid issues in Stream
- Parallelized using MPI
- Some common optimizations present
  - Fused collision-stream step for g
  - Neighbors calculated instead of read from array
  - Bidirectional MPI exchanges used
First Port to MIC

- Removed all MPI calls
- Included OMP in collision function
  - Most math is performed here
  - Takes 95% of run time on host
- Parallelized outermost loop (in z direction)
  - Innermost loop not broken – vectorization
  - Must be careful with number of threads
    - When using multiple threads per core, if \( \frac{z_{\text{max}}}{\text{OMP\_NUM\_THREADS}} \) not a multiple of the number of cores, performance will be degraded
- No vector hints used
First Port Results

MIC
- OMP_NUM_THREADS = 240
- KMP_AFFINITY = balanced,granularity=fine
- Performance
  - 7.7 MLUPS

CPU
- OMP_NUM_THREADS = 16
- KMP_AFFINITY = compact,granularity=fine
- Performance
  - 32.9 MLUPS

Domain Size = 240x240x240x240
Number of Iterations = 100
MLUPS = Millions of Lattice Updates Per Second

Disappointing!!
CPU is roughly 4X FASTER than MIC
WHY??
Finding the Hotspots

- Instrumented the code
- Timings revealed bottleneck moved from collision to stream
- Single thread on MIC too weak to achieve appropriate memory bandwidth
- Turns out profile from Host is misleading and does not predict behavior on the MIC
- Should have guessed that 😞

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<tr>
<th>Function</th>
<th>Time (sec)</th>
<th>% Run Time</th>
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<tbody>
<tr>
<td>Collision</td>
<td>44.4</td>
<td>24.8</td>
</tr>
<tr>
<td>PostCollision</td>
<td>1.1</td>
<td>0.6</td>
</tr>
<tr>
<td>Stream</td>
<td>123.2</td>
<td>68.9</td>
</tr>
<tr>
<td>PostStream</td>
<td>10.3</td>
<td>5.7</td>
</tr>
</tbody>
</table>
Fixing the Bandwidth Bottleneck

- Added OMP to all heavy data movement sections
  - PostCollision
  - Stream
  - PostStream
- Re-run test case with identical settings
- Stream function performance improved by factor 89x
- Bottleneck moved back to Collision
- Both MIC and CPU performance improved
  - MIC improved by 3.9x
  - CPU improved by 1.6x
- Smaller improvement on CPU due to heavier threads

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</tr>
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<td>PostCollision</td>
<td>0.03</td>
<td>0.1</td>
</tr>
<tr>
<td>Stream</td>
<td>1.4</td>
<td>3.0</td>
</tr>
<tr>
<td>PostStream</td>
<td>0.3</td>
<td>0.6</td>
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Performance (MIC) = 29.7 MLUPS
Performance (CPU) = 52.4 MLUPS
CPU is still FASTER by a factor 1.8x
What Could Be Missing?

- Adding OMP has only given us enough performance to roughly match a single Xeon E5 socket.
- Much of the performance of the MIC is achieved via the 512-bit vector width.
- We could be loosing up to a factor 8x in performance.
- It is time to look at the vectorization of the code.
Vector Reports

- Using the Intel compiler option -vec-report3 we find:

  collision.f90(40): (col. 6) remark: LOOP WAS VECTORIZED.
  collision.f90(40): (col. 6) remark: PEEL LOOP WAS VECTORIZED.
  collision.f90(40): (col. 6) remark: REMAINDER LOOP WAS VECTORIZED.
  collision.f90(39): (col. 4) remark: loop was not vectorized: not inner loop.
  collision.f90(38): (col. 2) remark: loop was not vectorized: not inner loop.
  collision.f90(51): (col. 6) remark: LOOP WAS VECTORIZED.
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  collision.f90(50): (col. 4) remark: loop was not vectorized: not inner loop.
  collision.f90(49): (col. 2) remark: loop was not vectorized: not inner loop.
  collision.f90(95): (col. 6) remark: loop was not vectorized: existence of vector dependence.
  collision.f90(164): (col. 4) remark: vector dependence: assumed FLOW dependence between lbparams_mp_g_line 164 and lbparams_mp_g_line 100.
  collision.f90(164): (col. 4) remark: vector dependence: assumed FLOW dependence between lbparams_mp_g_line 164 and lbparams_mp_g_line 117.
  collision.f90(164): (col. 4) remark: vector dependence: assumed FLOW dependence between lbparams_mp_g_line 164 and lbparams_mp_g_line 164.
  collision.f90(94): (col. 4) remark: loop was not vectorized: not inner loop.
  collision.f90(93): (col. 2) remark: loop was not vectorized: not inner loop.
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  collision.f90(93): (col. 2) remark: loop was not vectorized: not inner loop.

This is not good: Most of our math heavy operations are performed in the loop at line 95.
Testing Vectorization

- We compiled two versions of the code:
  -O3 -openmp -mmic
  -O3 -openmp -mmic -novec

- MIC Performance (vec) = 29.7 MLUPS

- MIC Performance (novec) = 27.9 MLUPS

- This merely confirms what the vector report told us: no vectorization in the main loop of collision.

- Using IVDEP directives did not change the result.

- Because of the use of doubly-buffered arrays there should not be a real data dependence in the loop

- But the compiler does not seem to realize this (changes during optimization?)
From AOS to SOA

\[
g(i, j, k, vel, buf) \rightarrow g_0(m), g_1(m), \ldots, g_{18}(m) \quad m = i + NX \cdot (j + NY \cdot k) + \text{offset}
\]

\[
f(i, j, k, vel, buf) \rightarrow f_0(m), f_1(m), \ldots, f_6(m) \quad m = i + NX \cdot (j + NY \cdot k) + \text{offset}
\]

- This maintains a doubly-buffered array but in a much simpler form
- Compiler is able to vectorize the main collision loop (-vec-report3)
- MIC performance increases by 3.3x to 127.7 MLUPS
- CPU performance decreases 4% to 50.1 MLUPS
- MIC is now 2.5x FASTER than a dual socket CPU node
KMP_AFFINITY and OMP scaling

SCALING AND AFFINITY
Binding Threads to Hardware

- Using the Intel KMP AFFINITY interface
  - KMP_AFFINITY={compact, scatter, balanced}
  - KMP_AFFINITY=explicit, proclist=[0,1,2,3]
  - Adding verbose will dump the full affinity information when the run starts
  - Adding granularity=fine binds to specific thread contexts and may help in codes with heavy L1 cache reuse

- The MIC is a single chip, so there is no need for numactl

- We run all tests with granularity=fine in order to prevent thread migration
KMP_AFFINITY Example

compact

balanced

scatter
Scaling for Different Affinity Settings

![Graph showing MLUPS vs Number of OMP Threads for different affinity settings: Balanced, Scatter, and Compact. The graph indicates different performance behaviors for each setting.](image-url)
OMP + Offload

HOST + COPROCESSOR EXECUTION
Code Design

- Workload division
  - Partitioning in the Y direction
  - Avoids shortening the vectorizable innermost loop
  - Avoids having unaligned accesses due to uncommon partition in the Z direction
  - Avoids reducing maximum number of usable threads (mapped to Z direction blocks)

- Data transfer
  - Unlike CUDA codes the default is not for data to be persistent on the coprocessors in between offload sections
  - Carefully annotated data transfers to avoid MIC reallocation
  - Using asynchronous transfers is a requirement for host + MIC execution in this mode

- There are CPU and MIC versions of each function
Offload Data Transfer Examples

Some definitions to help handle transfers:

#define ALLOC alloc_if(.TRUE.)
#define REUSE alloc_if(.FALSE.)
#define FREE free_if(.TRUE.)
#define KEEP free_if(.FALSE.)

Transfer to mic device with id 0, allocating the data on the MIC, copying it over and returnign to the host without freeing the array:

!DIR$ OFFLOAD_TRANSFER TARGET(MIC:0) IN( buff_mic : ALLOC KEEP )

Offload function PostCollisionMIC, reuse current values of array on device mic 0 during offload and return array values to host when offload is completed without freeing the array:

!DIR$ OFFLOAD BEGIN TARGET(MIC:0) OUT(buff_mic : REUSE KEEP )
   CALL PostCollisionMIC
!DIR$ END OFFLOAD
Offload Data Transfers

![Graph showing bandwidth vs. message size for ALLOC/FREE and REUSE/KEEP](graph.png)
Host + Coprocessor Results

- Since native execution is roughly 2.5x faster on the mic a naïve partition is 2.5 / (2.5 + 1) = 0.71 (71% workload for MIC)
- Tried in the range 60% - 80%, and optimal performance was found for 70% MIC workload
- MIC+CPU performance is 142.8 MLUPS
- Equivalent to 2.8 CPU nodes (44 CPU cores)
- Performance is relatively good, but this code had several issues
  - Not scalable (one node only)
  - Time consuming because of (essentially) duplicated functions
  - Increased development errors due to larger number of functions
MPI+OMP

SYMMETRIC EXECUTION
Code Design

- MPI partitioning allowed in 3D
  - But restricted to Y when possible to maximize length of innermost loop (vectorization) and length of outermost loop (OMP)
- MPI calls are made inside OMP MASTER regions
- MPI and OMP unaware of each other
- MPI exchanges are performed in PostCollision and PostStream
- Single ghost layer (or halo) used for MPI data exchange
- Load balance is coarse-grained
  - It depends on the number of tasks assigned to CPU and MIC
- No need to duplicate functions
- Requires two binaries
- Initially worried about MPI MIC to CPU data exchange
  - 5x slower than CPU to MIC
  - Fixed in latest Mvapich2
MIC/Host MPI Exchanges

Intel MPI

Mvapich2
Symmetric Execution Results

- We used 2 tasks on the MIC and 1 task on the CPU to assign a 66% workload fraction to the MIC.

- The number of threads was 16 for the CPU and 120 for each of the MIC tasks.

- Measured performance was 147.0 MLUPS.

- This is equivalent to 2.8x nodes using only the CPUs.

- This code design is scalable, and required only one major code change (the AOS to SOA modification).
Performance and Code Evolution

The chart illustrates the performance (in MLUPS) for different code versions and configurations:

- **CPU**
- **MIC**
- **CPU+MIC**

The categories compared are:

- OMP_v1
- OMP_v2
- SOA
- Offload
- Symmetric

The diagram shows a significant performance difference between the configurations, with Symmetric and Offload performing the best.
Summary

- Initial port of a multiphase LBM code to the MIC yielded low performance
  - 4x slower than a CPU node

- Final performance is very satisfactory for the amount of work performed
  - 2.8x faster than a cpu node alone

- Host profiles were not useful when porting

- There are some poorly understood alignment issues

- SOA + Symmetric execution mode provide good performance and scalability potential
FDTD Case Study -- ICT
Finite Difference Time Domain

Application background

- Widely used in many electromagnetics domains

Microwave

Electromagnetic detection

Radar

electromagnetic protection

Navigation

Antenna
Finite Difference Time Domain

Algorithm introduction

• An algorithm used for electromagnetic simulation by solving Maxwell equation.

\[
\begin{align*}
\nabla \times E &= -\mu \frac{\partial H}{\partial t} \\
\nabla \times H &= \epsilon \frac{\partial E}{\partial t} + \sigma E
\end{align*}
\]

For example, \( E_x \) obtained by:

\[
E_x^{n+1}(i+1/2, j, k) = \frac{2\epsilon(m) - \sigma(m)\Delta t}{2\epsilon(m) + \sigma(m)\Delta t} E_x^n(i+1/2, j, k) + \frac{2\Delta t}{2\epsilon(m) + \sigma(m)\Delta t} \left[ H_y^{n+1/2}(i+1/2, j+1/2, k) - H_y^{n+1/2}(i+1/2, j-1/2, k) \right] / \Delta y
\]

\[
H_y^{n+1/2}(i+1/2, j, k+1/2) - H_y^{n+1/2}(i+1/2, j, k-1/2) / \Delta z
\]
Hotspot Analysis

- Define the candidate functions for optimization
  - update_E_PML (21.5%), update_H_PML (24.7%)
  - update_e (18.8% CPU time), update_h (19.1%)

Grid initialization

Analyses input, initial conditions

Meet iteration condition(s)?

YES
  - Update E
  - Update E_PML
  - Update H
  - Update H_PML
  - output
  - END

NO
Scalability Optimization

- Scalability was improved a lot compared to the baseline code after optimization by
  - Loop fusion
  - Merge the nested loop

```c
#pragma omp for nowait
for(i=0; i <= nx; i++)
  for(j=1; j <= ny; j++)
    for(k=1; k <= nz; k++) {
      .......
    }

int j_end = ny+1;
int ij_end = (nx+1)*(ny+1);
int ij_start = j_end + 1;
#pragma omp for nowait
for(int ij=ij_start; ij < ij_end; ij++) {
  i = ij/j_end;
  j = ij%j_end;
  if(!j) continue;
  for(k=1; k <= nz; k++) {
    .......
  }
```

```c
#pragma omp for nowait
for(i=0; i <= nx; i++)
  for(j=1; j <= ny; j++)
    for(k=1; k <= nz; k++) {
      Ex = .......
    }
#pragma omp for nowait
for(i=0; i <= nx; i++)
  for(j=1; j <= ny; j++)
    for(k=1; k <= nz; k++) {
      Ey = .......
    }
#pragma omp for nowait
for(i=0; i <= nx; i++)
  for(j=1; j <= ny; j++)
    for(k=1; k <= nz; k++) {
      Ez = .......
      Ex = .......
      Ey = .......
      Ez = .......
    }
```
Vectorization

• Compiler help to auto-vectorize the most inner loop by
  - Remove code dependency
  - #pragma simd
  - Adding compiler option "-ansi-alias"
• Check the speed up of scalar code vs vectorized code

Vectorization on SNB

Vectorization on KNC
Implement on Intel® Xeon Phi™ coprocessor

• Written by C and paralleled by OpenMP.

• Include three computation dataset mode, the performance shows different: small, medium, large dataset

• Migration to Intel® MIC in native mode, with medium dataset. (240*300*300)

• The optimized performance shows below,

![Graph showing speedup over baseline code on E5-2670]

<table>
<thead>
<tr>
<th>SNB</th>
<th>KNC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual E5–2670</td>
<td>61 cores</td>
</tr>
<tr>
<td>2.6GHz</td>
<td>1.09 GHz</td>
</tr>
<tr>
<td>Memory size: 8GB</td>
<td></td>
</tr>
<tr>
<td>Compiler XE 13 0.079</td>
<td>Compiler XE 13 0.079</td>
</tr>
</tbody>
</table>
Case Study: Deep Learning
Case Study on IPDC

- Case: Deep Learning
  - Deep Learning is a new domain of machine learning, it uses multiple layers of nonlinear neural network instead of traditional static models.
  - Deep Learning brings subversive influence to human-machine interaction technology such as voice, image, handwriting, and so on.
  - Deep Learning greatly improves accuracy and processing time.
  - Deep Learning is also a time-consuming part in model training.
Hotspots Analysis

- 2S SNB Baseline: no optimization, single thread, time: 77.33s
- Hardware: 2Sockets Intel® Xeon E5-2670 (8 cores, 2.6GHz)
- Most time consuming function is ContrastiveDivergence: self time 69.8s, 90%
- CPI = 5.6 too high
Hotspots Analysis

• L1 cache hit ratio: $\frac{2640}{24978} = 10.6\%$, too low

<table>
<thead>
<tr>
<th>Hardware Event Type</th>
<th>Hardware Event Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_CLK_UNHALTED.THREAD</td>
<td>201,778,000,000</td>
</tr>
<tr>
<td>MEM_LOAD_UOPS_LLC_HIT RETIRED.XSNP_HITM</td>
<td>300,000</td>
</tr>
<tr>
<td>MEM_LOAD_UOPS_LLC_HIT RETIRED.XSNP_HIT</td>
<td>0</td>
</tr>
<tr>
<td>MEM_LOAD_UOPS_LLC_HIT RETIRED.XSNP_MISS</td>
<td>0</td>
</tr>
<tr>
<td>MEM_LOAD_UOPS_LLC_HIT RETIRED.XSNP_NONE</td>
<td>19,239,000,000</td>
</tr>
<tr>
<td>MEM_LOAD_UOPS RETIRED.LLC_MISS</td>
<td>32,760,000</td>
</tr>
<tr>
<td>MEM_LOAD_UOPS RETIRED.HIT_LFB_PS</td>
<td>3,122,700,000</td>
</tr>
<tr>
<td>MEM_LOAD_UOPS RETIRED.L1_HIT_PS</td>
<td>2,640,000,000</td>
</tr>
<tr>
<td>MEM_LOAD_UOPS RETIRED.L2_HIT_PS</td>
<td>21,600,000</td>
</tr>
<tr>
<td>MEM_UOPS RETIRED.ALL LOADS_PS</td>
<td>24,978,000,000</td>
</tr>
<tr>
<td>MEM_UOPS RETIRED.ALL STORES_PS</td>
<td>702,000,000</td>
</tr>
</tbody>
</table>
Optimization on Intel Xeon

- Original code
  - Inconsecutive access in innermost loop, blocking vectorization and cache hits

```c
for (i = 0; i < I; i++)
{
    for (s = 0; s < samples/Rows*/s++)
    {
        delta += v[s*I + i]*h_data[s*J + j] - v_rec0[s*I + i]*h_rec0[s*J + j]
    }
    delta /= samples;
    w[j*I + i] = w[j*I + i] + momentum * lastDeltaW[j*I + i] + 0.004 * delta;
    lastDeltaW[j*I + i] = 0.004 * delta + momentum * lastDeltaW[j*I + i];
}

float deltaB = (0.0);
for (s = 0; s < samples/Rows*/s++)
{
    deltaB += h_data[s*J + j] - h_rec0[s*J + j];
}
```

Inconsecutive access
Optimization on Intel Xeon

- Optimization V1
  - transpose for consecutive access in innermost loop
  - SIMD optimization

```c
for (s = 0; s < samples; s++)
{
    for (i = 0; i < I; i++)
    {
        v_trs[i * samples + s] = v[s * I + i];
        v_recon_trs[j * samples + s] = v_recon[s * I + j];
    }

    for (j = 0; j < J; j++)
    {
        h_data_trs[j * samples + s] = h_data[s * I + j];
        h_recon_trs[j * samples + s] = h_recon[s * I + j];
    }
}

#define OPT1
#if defined USE_PRAG_SIMD
#pragma loop_count=DS
#pragma simd reduction(+:delta)
#endif

for (s = 0; s < samples/(*v->rows())); s++)
{
    ifndef OPT1
        delta += v[s * I + i] * h_data[s * J + j] - v_recon[s * I + i] * h_recon[s * J + j];
    else
        //delta += v_trs[j * samples + s] * h_data_trs[j * samples + s] - v_recon_trs[j * samples + s] * h_recon_trs[j * samples + s];
        delta += v_trs_ptr[s] * h_data_trs_ptr[s] - v_recon_trs_ptr[s] * h_recon_trs_ptr[s];
    #endif
}
```
Optimization on Intel Xeon

• Original code
  - Inconsecutive access in innermost loop, blocking vectorization and cache hits

```c
for (s = 0; s < samples; s++)
{
    for (i = 0; i < I; i++)
    {
        float sum = a[i];
        for (j = 0; j < J; j++)
        {
            sum += h[s * J + j] * v[j * I + i];
        }
    }
    v[s * I + i] = sum;
}
```
Optimization on Intel Xeon

- Optimization V2
  - Reconstruction code, directly write to result array and exchange outer loops
  - SIMD optimization

```c
for (s = 0; s < samples; s++)
{
    memcpy(v + s * I, a, I * sizeof(float));
    for (j = 0; j < J; j++)
    {
        if (USE_PRAG_SIMD)
        {
            #pragma loop_count=DS
            #pragma simd
            
            for (i = 0; i < I; i++)
            {
                v[s * I + i] += h[s * J + j] * w[j * I + i];
            }
        }
    }
}
```
Optimization on Intel Xeon

- Optimization V3
  - Reconstruct code, split the value assigning to a different loop
  - Left codes can use MKL sgemm, which has been highly optimized both on Intel Xeon and Intel Xeon Phi

```c
for (s = 0; s < samples; s++)
{
    memcpy(v + s * I, a, I * sizeof(float));
    for (j = 0; j < J; j++)
    {
        ifdef USE_PRAG_SIMD
#define loop_count=DS
#pragma simd
#endif
        for(i = 0; i < I; i++)
        {
            v[s * I + i] += h[s * J + j] * w[j * I + i];
        }
    }
}
for (s = 0; s < samples; s++)
{
    memcpy(v + s * I, a, I * sizeof(float));
    cblas_sgemm(CblasRowMajor, CblasNoTrans, CblasNoTrans,
                samples, I, J, 1.0f, h, J, w, I, 1.0f, v, I);
```
Optimization on Intel Xeon

- **Optimization V4**
  - Use OpenMP multi-threads to scale code to multi/many cores
  - Use schedule(dynamic) to ensure load balance between different threads
  - Use KMP_AFFINITY=balanced,granularity=thread to bind threads to multi/many cores, avoiding threads migration

```c
#ifdef USE_MULTITHREADS
#ifdef __MIC__
#pragma omp parallel for private(j) schedule(dynamic, OMP_GRAIN) num_threads(NUM_THREADS)
#else
#pragma omp parallel for private(j) schedule(dynamic, OMP_GRAIN) num_threads(NUM_THREADS)
#endif
#endif

for (j = 0; j < J; j++)
{
#ifdef OPT1
    float *h_data_trs_ptr = h_data_trs + j * samples;
    float *h_recon_trs_ptr = h_recon_trs + j * samples;
#endif

    float deltaB = (0.0f);

#ifdef USE_PRAG_SIMD
#pragma loop_count=DS
#pragma simd reduction(+:deltaB)
#endif
    for (int s = 0; s < samples/(*v->Rows())/; s++)
    {
#ifdef OPT1
        deltaB += h_data[s * J + j] - h_recon[s * J + j];
#else
        //deltaB += h_data_trs[j * samples + s] - h_recon_trs[j * samples + s];
        deltaB += h_data_trs_ptr[s] - h_recon_trs_ptr[s];
#endif
    }
}
```
Optimization on Intel Xeon

- Optimization V5
  - Original code
  - Glibc rand() is not thread safe function, and will block parallelism

```c
for (s = 0; s < samples; s++)
{
    for (j = 0; j < J; j++)
    {
        float *v_ptr = v + s * I;
        float *w_ptr = w + j * I;
        float sum = b[j];

        #ifdef USE_PRAG_SIMD
        #pragma loop_count=DI
        #pragma simd reduction(+:sum)
        #endif

        for(i = 0; i < I; i++)
        {
            //sum += v[s * I + i] * w[j * I + i];
            sum += v_ptr[i] * w_ptr[i];
        }

        //h[s * J + j] = CUDA_SIGMOID(sum);
        h[s * J + j] = 1/(1.0f+expf(sum));
        h_recon[s * J + j] = (h[s * J + j] > ((float)rand()/RAND_MAX))? 1.0f:0.0f;
    }
}
```
Optimization on Intel Xeon

- Optimization V5
  - Original code
  - Glibc rand() is not thread safe function, and will block parallelism

```c
for (s = 0; s < samples; s++)
{
    for (j = 0; j < J; j++)
    {
        float *v_ptr = v + s * I;
        float *w_ptr = w + j * I;
        float sum = b[j];

        #ifdef USE_PRAGSIMD
        #pragma loop_count=DI
        #pragma simd reduction(+:sum)
        #endif

        for(i = 0; i < I; i++)
        {
            //sum += v[s * I + i] * w[j * I + i];
            sum += v_ptr[i] * w_ptr[i];
        }

        //h[s * J + j] = CUDA_SIGMOID(sum);
        h[s * J + j] = 1/(1.0f+expf(sum));
        h_recon[s * J + j] = (h[s * J + j] < ((float)rand()/RAND_MAX)) ? 1.0f:0.0f;
    }
}
```
Optimization on Intel Xeon

- Optimization V5
  - Pre-calculate rand()
  - Increasing parallelism

```c
#pragma omp parallel for private(s, j) collapse(2) schedule(dynamic) num_threads(NUM_THREADS)
for (s = 0; s < samples; s++)
{
    for (j = 0; j < J; j++)
    {
        float *v_ptr = v + s * I;
        float *w_ptr = w + j * I;
        float sum = b[j];
        #ifdef USE_PRAG_SIMD
        #pragma loop_count=DI
        #pragma simd reduction(+:sum)
        #endif
        for (i = 0; i < I; i++)
        {
            //sum += v[s * I + i] * w[j * I + i];
            sum += v_ptr[i] * w_ptr[i];
            //h[s * J + j] = CUDA_SIGMOID(sum);
            h[s * J + j] = 1/(1.0f+expf(sum));
    h_recon[s * J + j] = (h[s * J + j] > rand_array[s * J + j] /((float)rand() / RAND_MAX)) ? 1.0f : 0.0f;
```
Optimization on Intel Xeon

• Optimization V6
  - Use MKL random generator instead of Glibc rand(), further increasing parallelism

```c
#define USE_MKL_RAND

vslNewStream(&Randomstream, /*VSL_BRNG_MT19937*/VSL_BRNG_SFMT19937, RANDSEED);
#endif

#ifndef USE_MKL_RAND

vsRngUniform (VSL_RNG_METHOD_UNIFORM_STD, Randomstream, samples * J, rand_array, 0.0f, 1.0f);
#endif

#else

for (s = 0; s < samples; s++)
{
    for (j = 0; j < J; j++)
    {
#endif

    #ifndef OPT7

    rand_array[s * J + j] = (float)rand() / RAND_MAX;
    #else

    rand_array[s * J + j] = (float)rand() * rcp_randmax;
    #endif

```
Optimization on Intel Xeon

- Optimization result on Intel Xeon
  - CPI reduced from 5.6 to 1.09
  - L1 cache hit ratio increased from 10.6% to 98.16%
  - Optimizations on Intel Xeon are all useful for Intel Xeon Phi

![Speedup vs. Original 1 thread](chart.png)
## Performance on Intel Xeon & Intel Xeon Phi

<table>
<thead>
<tr>
<th></th>
<th>Xeon® E5 processor – 1 threads baseline</th>
<th>Xeon® E5 processor – 32 threads optimization</th>
<th>Xeon Phi ™ coprocessor – 244 tasks optimization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time elapsed</td>
<td>77.335 s</td>
<td>0.2162 s</td>
<td>0.085 s</td>
</tr>
</tbody>
</table>

**SNB:** 2S Intel® Xeon E5-2670 (8 cores, 2.6GHz)
**MIC:** Intel® Xeon Phi™ (B0, 61 cores, 1.1GHz; 8GB @ 5.5GT/s)

### Speedups vs. SNB Original 1 thread

- Original 1 thread: 1.00
- 2S SNB Optimization 32 threads: 357.70
- 1 MIC Optimization 244 threads: 910.90

*Speedup*
英特尔®软件学院2013年全新推出的课程
基于英特尔®集成众核架构的编程和优化

授课形式：课堂讲授+动手实验

课程长度：2-4天（可基于客户需求定制）

目标学员：
本课程适合集群和并行系统设计高性能，可扩充应用的软件工程师，项目负责人和解决方案架构师；计算机、高性能应用相关专业的教师等。

课程描述：
本课程总时长为期4天，采用课堂授课与动手实践相结合的方式，主要内容包括英特尔集成众核架构介绍，基于众核架构的开发环境搭建、众核编程、调试、优化以及实际应用案例分享等。本课程设计根据不同用户需求，由初级、中级、高级三部分组成，学生们可以从中阶梯式地学习和掌握课程内容。重点在于了解如何将实际应用移植到集成众核架构，利用英特尔®工具分析并提取应用特征，通过多线程、多任务、向量化等并行优化方法获得性能提升。案例研究说明如何将课堂上的方法和工具合理配合，提升实际应用的性能。
培训模式及联系方式

英特尔®软件学院

VIP客户/MIC培训中心

英特尔®软件学院

MIC培训中心

客户

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Backup